

NB7L86M

2.5V/3.3V 12 Gb/s Differential Clock/Data SmartGate with CML Output and Internal Termination

The NB7L86M is a multi-function differential Logic Gate, which can be configured as an AND/NAND, OR/NOR, XOR/XNOR, or 2:1 MUX. This device is part of the GigaComm family of high performance Silicon Germanium products. The NB7L86M is an ultra-low jitter multi-logic gate with a maximum data rate of 12 Gb/s and input clock frequency of 8 GHz suitable for Data Communication Systems, Telecom Systems, Fiber Channel, and GigE applications.

Differential inputs incorporate internal 50 Ω termination resistors and accept LVNECL (Negative ECL), LVPECL (Positive ECL), LVCMOS, LVTTTL, CML, or LVDS. The differential 16 mA CML output provides matching internal 50 Ω termination, and 400 mV output swing when externally terminated 50 Ω to VCC.

The device is housed in a low profile 3x3 mm 16-pin QFN package.

Application notes, models, and support documentation are available on www.onsemi.com.

Features

- Maximum Input Clock Frequency up to 8 GHz
- Maximum Input Data Rate up to 12 Gb/s Typical
- < 0.5 ps of RMS Clock Jitter
- < 10 ps of Data Dependent Jitter
- 30 ps Typical Rise and Fall Times
- 90 ps Typical Propagation Delay
- 2 ps Typical Within Device Skew
- Operating Range: V_{CC} = 2.375 V to 3.465 V with V_{EE} = 0 V
- CML Output Level (400 mV Peak-to-Peak Output) Differential Output
- 50 Ω Internal Input and Output Termination Resistors
- Functionally Compatible with Existing 2.5 V/3.3 V LVEL, LVEP, EP and SG Devices
- Pb-Free Packages are Available

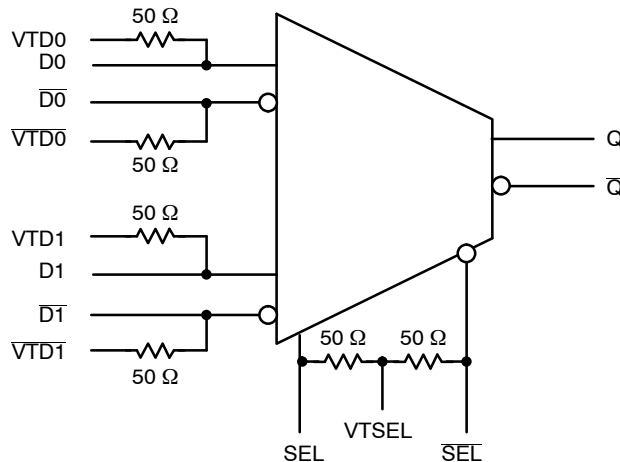


Figure 1. Simplified Logic Diagram



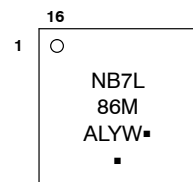
ON Semiconductor®

<http://onsemi.com>



QFN16
MN SUFFIX
CASE 485G

MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

NB7L86M

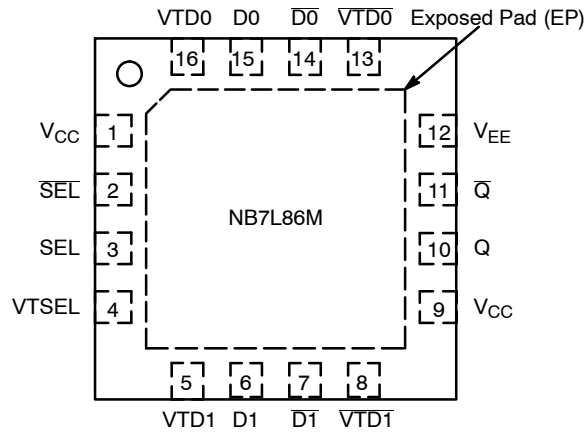


Figure 2. Pin Configuration (Top View)

Table 1. PIN DESCRIPTION

| Pin | Name | I/O | Description |
|------|--------------------------|---|---|
| 1, 9 | V _{CC} | Power Supply | Positive supply voltage. All V _{CC} pins must be externally connected to power supply to guarantee proper operation. |
| 2 | $\overline{\text{SEL}}$ | LVPECL, CML, LVCMOS, LVTTTL, LVDS Input | Inverted differential select logic input. |
| 3 | SEL | LVPECL, CML, LVCMOS, LVTTTL, LVDS Input | Non-inverted differential select logic Input. |
| 4 | V _{TSEL} | - | Common internal 50 Ω termination pin for SEL/ $\overline{\text{SEL}}$. See Table 6. (Note 1) |
| 5 | V _{TD1} | - | Internal 50 Ω termination pin for D1. See Table 6. (Note 1) |
| 6 | D1 | LVPECL, CML, LVCMOS, LVTTTL, LVDS Input | Non-inverted differential clock/data input D1. (Note 1) |
| 7 | $\overline{\text{D1}}$ | LVPECL, CML, LVCMOS, LVTTTL, LVDS Input | Inverted differential clock/data input $\overline{\text{D1}}$. (Note 1) |
| 8 | $\overline{\text{VTD1}}$ | - | Internal 50 Ω termination pin for $\overline{\text{D1}}$. See Table 6. (Note 1) |
| 10 | Q | CML Output | Non-inverted output with internal 50 Ω source termination resistor. (Note 2) |
| 11 | $\overline{\text{Q}}$ | CML Output | Inverted output with internal 50 Ω source termination resistor. (Note 2) |
| 12 | V _{EE} | Power Supply | Negative supply voltage. All V _{EE} pins must be externally connected to power supply to guarantee proper operation. |
| 13 | $\overline{\text{VTD0}}$ | - | Internal 50 Ω termination pin for D0. (Note 1) |
| 14 | $\overline{\text{D0}}$ | LVPECL, CML, LVCMOS, LVTTTL, LVDS Input | Non-inverted differential clock/data input $\overline{\text{D0}}$. (Note 1) |
| 15 | D0 | LVPECL, CML, LVCMOS, LVTTTL, LVDS Input | Non-inverted differential clock/data input D0. (Note 1) |
| 16 | V _{TD0} | - | Internal 50 Ω termination pin for $\overline{\text{D0}}$. (Note 1) |
| - | EP | - | Exposed Pad. Thermal pad on the package bottom must be attached to a heatsinking conduit to improve heat transfer. It is recommended to connect the EP to the lower potential (V _{EE}). |

1. In the differential configuration when the input termination pins (V_{TDx}, $\overline{\text{VTDx}}$, V_{TSEL}) are connected to a common termination voltage or left open, and if no signal is applied on Dx, $\overline{\text{Dx}}$, SEL and $\overline{\text{SEL}}$ then the device will be susceptible to self-oscillation.
2. CML output require 50 Ω receiver termination resistor to V_{CC} for proper operation.

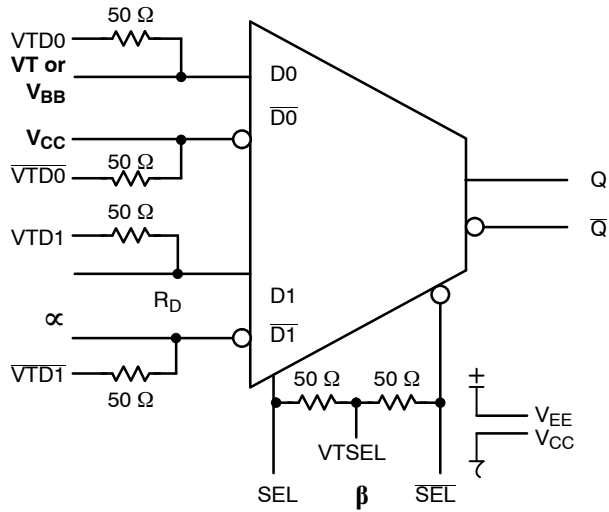


Figure 3. Configuration for AND/NAND Function

Table 2. AND/NAND TRUTH TABLE (Note 3)

| | ∞ | b | ∞ AND b |
|----|----------|-----|----------------|
| D0 | D1 | SEL | Q |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |

3. $\overline{D0}$, $\overline{D1}$, \overline{SEL} are complementary of D0, D1, SEL unless specified otherwise.

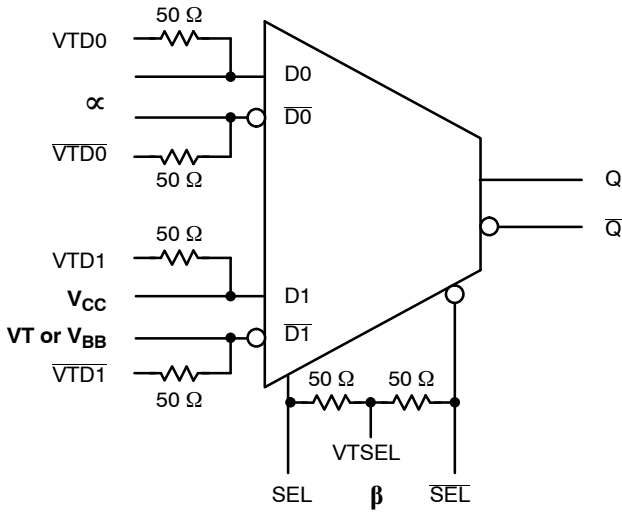


Figure 4. Configuration for OR/NOR Function

Table 3. OR/NOR TRUTH TABLE (Note 4)

| ∞ | | β | ∞ or β |
|----------|----|---------|---------------------|
| D0 | D1 | SEL | Q |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

4. $\overline{D0}$, $\overline{D1}$, \overline{SEL} are complementary of D0, D1, SEL unless specified otherwise.

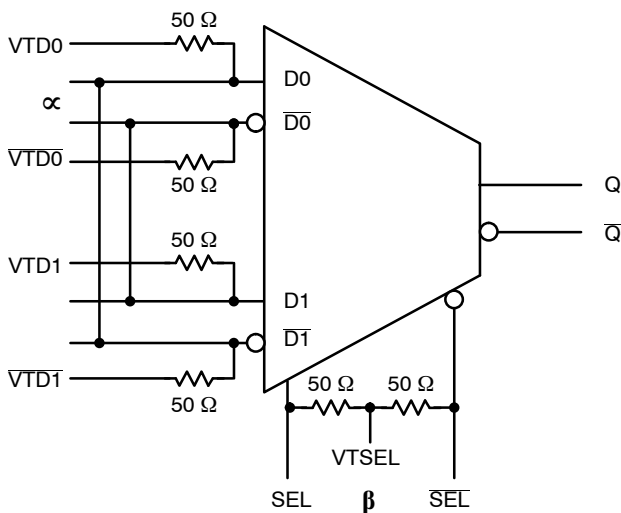


Figure 5. Configuration for XOR/XNOR Function

Table 4. XOR/XNOR TRUTH TABLE (Note 5)

| ∞ | | β | ∞ XOR β |
|----------|----|---------|----------------------|
| D0 | D1 | SEL | Q |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |

5. $\overline{D0}$, $\overline{D1}$, \overline{SEL} are complementary of D0, D1, SEL unless specified otherwise.

NB7L86M

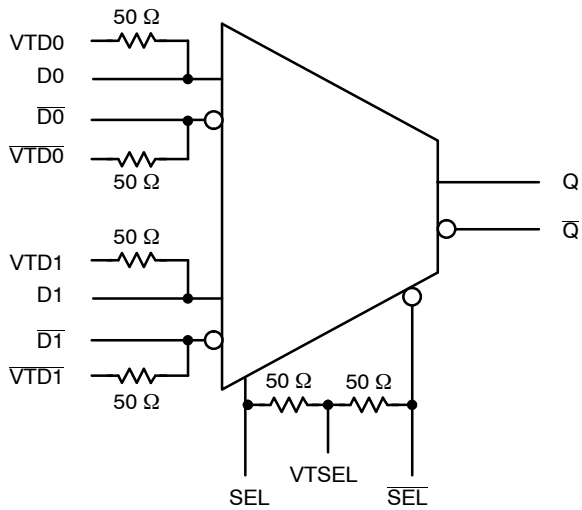


Figure 6. Configuration for 2:1 MUX Function

Table 5. 2:1 MUX TRUTH TABLE (Note 6)

| SEL | Q |
|-----|----|
| 1 | D1 |
| 0 | D0 |

6. D0, D1, SEL are complementary of D0, D1, SEL unless specified otherwise.

Table 6. ATTRIBUTES

| Characteristics | | Value | |
|--|------------------------|----------------------|-------------|
| ESD Protection | Human Body Model | > 1500 V | |
| | Machine Model | > 50 V | |
| | Charged Device Model | > 500 V | |
| Moisture Sensitivity (Note 7) | | Pb Pkg | Pb-Free Pkg |
| | QFN-16 | Level 1 | Level 1 |
| Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in | |
| Transistor Count | | 400 | |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | | |

7. For additional Moisture Sensitivity information, refer to Application Note AND8003/D.

Table 7. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Units |
|-------------------|--|--|--|---|--------------|
| V _{CC} | Positive Power Supply | V _{EE} = 0 V | | 3.6 | V |
| V _I | Input Voltage | V _{EE} = 0 V | V _{EE} ≤ V _I ≤ V _{CC} | 3.6 | V |
| V _{INPP} | Differential Input Voltage D - D̄ | V _{CC} - V _{EE} ≥ 2.8 V V _{CC} - V _{EE} < 2.8 V | | 2.8 V _{CC} - V _{EE} | V V |
| I _{IN} | Input Current Through R _T (50 Ω Resistor) | Continuous Surge | | 25 50 | mA mA |
| I _{out} | Output Current | Continuous Surge | | 25 50 | mA mA |
| T _A | Operating Temperature Range | QFN-16 | | -40 to +85 | °C |
| T _{stg} | Storage Temperature Range | | | -65 to +150 | °C |
| θ _{JA} | Thermal Resistance (Junction-to-Ambient) (Note 8) | 0 lfpm 500 lfpm | QFN-16 QFN-16 | 42 36 | °C/W °C/W |
| θ _{JC} | Thermal Resistance (Junction-to-Case) | 2S2P (Note 8) | QFN-16 | 3 to 4 | °C/W |
| T _{sol} | Wave Solder | Pb Pb-Free | | 265 265 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

8. JEDEC standard multilayer board - 2S2P (2 signal, 2 power).

NB7L86M

Table 8. DC CHARACTERISTICS ($V_{CC} = 2.375 \text{ V to } 3.465 \text{ V}$, $V_{EE} = 0 \text{ V}$, $T_A = -40^\circ\text{C to } +85^\circ\text{C}$)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|----------|--|----------------|----------------|----------------|------|
| I_{CC} | Power Supply Current (Inputs and Outputs Open) | | 38 | 50 | mA |
| V_{OH} | Output HIGH Voltage (Notes 9 and 10) | $V_{CC} - 60$ | $V_{CC} - 30$ | V_{CC} | mV |
| V_{OL} | Output LOW Voltage (Notes 9 and 10) | $V_{CC} - 460$ | $V_{CC} - 400$ | $V_{CC} - 310$ | mV |

Differential Input Driven Single-Ended (see Figures 16 & 18)

| | | | | | |
|----------|---|---------------|--|----------------|----|
| V_{th} | Input Threshold Reference Voltage Range (Note 11) | 1125 | | $V_{CC} - 75$ | mV |
| V_{IH} | Single-ended Input HIGH Voltage (Note 12) | $V_{th} + 75$ | | V_{CC} | mV |
| V_{IL} | Single-ended Input LOW Voltage (Note 12) | V_{EE} | | $V_{CC} - 150$ | mV |

Differential Inputs Driven Differentially (see Figures 17 & 19)

| | | | | | | |
|------------------|---|---------------------------|------------|---------------|------------|----|
| V_{IHD} | Differential Input HIGH Voltage | 1200 | | V_{CC} | mV | |
| V_{ILD} | Differential Input LOW Voltage | V_{EE} | | $V_{CC} - 75$ | mV | |
| V_{CMR} | Input Common Mode Range (Differential Configuration) | 1163 | | $V_{CC} - 38$ | mV | |
| V_{ID} | Differential Input Voltage ($V_{IHD} - V_{ILD}$) | 75 | | 2500 | mV | |
| I_{IH} | Input HIGH Current | D0/D0̄/D1/D1̄ SEL/SEL̄ | 0 0 | 50 20 | 150 150 | μA |
| I_{IL} | Input LOW Current | D0/D0̄/D1/D1̄ SEL/SEL̄ | -50 -50 | 50 20 | 100 100 | μA |
| R_{TIN} | Internal Input Termination Resistor | 45 | 50 | 55 | Ω | |
| R_{TOUT} | Internal Output Termination Resistor | 45 | 50 | 55 | Ω | |
| $R_{Temp\ Coef}$ | Internal I/O Termination Resistor Temperature Coefficient | | 6.38 | | mΩ/°C | |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range.

Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

9. CML outputs require 50 Ω receiver termination resistors to V_{CC} for proper operation.

10. Input and output parameters vary 1:1 with V_{CC} .

11. V_{th} is applied to the complementary input when operating in single-ended mode.

12. V_{CMR} min varies 1:1 with V_{EE} , V_{CMR} max varies 1:1 with V_{CC} .

NB7L86M

Table 9. AC CHARACTERISTICS ($V_{CC} = 2.375 \text{ V}$ to 3.465 V , $V_{EE} = 0 \text{ V}$; Note 13)

| Symbol | Characteristic | -40° C | | | 25° C | | | 85° C | | | Unit |
|--------------------------|--|------------|--------------------------|-------------------------|------------|--------------------------|-------------------------|------------|--------------------------|-------------------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| V_{OUTPP} | Output Voltage Amplitude (@ $V_{INPPmin}$) (See Figure 7) $f_{in} \leq 4 \text{ GHz}$ $f_{in} \leq 8 \text{ GHz}$ | 240 125 | 350 230 | | 240 125 | 350 230 | | 240 125 | 350 230 | | mV |
| f_{data} | Maximum Operating Data Rate | 10.7 | 12 | | 10.7 | 12 | | 10.7 | 12 | | Gb/s |
| t_{PLH} , t_{PHL} | Propagation Delay to Output Differential @ 1 GHz (See Figure 7) Dx/\overline{Dx} to Q/\overline{Q} SEL/\overline{SEL} to Q/\overline{Q} | 70 110 | 90 135 | 120 180 | 70 110 | 90 135 | 120 180 | 70 110 | 90 135 | 120 180 | ps |
| t_{SKEW} | Duty Cycle Skew (Note 14) Device-to-Device Skew (Note 15) | | 2.0 5.0 | 10 20 | | 2.0 5.0 | 10 20 | | 2.0 5.0 | 10 20 | ps |
| t_{JITTER} | RMS Random Clock Jitter (Note 16) Peak/Peak Data Dependent Jitter (Note 17) $f_{in} = 4 \text{ GHz}$ $f_{in} = 8 \text{ GHz}$ $f_{data} = 5 \text{ Gb/s}$ $f_{data} = 10 \text{ Gb/s}$ | | 0.2 0.2 2.0 4.0 | 0.5 0.5 8.0 10 | | 0.2 0.2 2.0 4.0 | 0.5 0.5 8.0 10 | | 0.2 0.2 2.0 4.0 | 0.5 0.5 8.0 10 | ps |
| V_{INPP} | Input Voltage Swing/Sensitivity (Differential Configuration) (Note 18) | 75 | 400 | 2500 | 75 | 400 | 2500 | 75 | 400 | 2500 | mV |
| t_r , t_f | Output Rise/Fall Times @ 1 GHz (20% - 80%) Q, \overline{Q} | | 35 | 60 | | 35 | 60 | | 35 | 60 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

13. Measured by forcing V_{INPP} (TYP) from a 50% duty cycle clock source. All loading with an external $R_L = 50 \Omega$ to V_{CC} . Input edge rates 40 ps (20% - 80%).
14. Duty cycle skew is measured between differential outputs using the deviations of the sum of T_{pw-} and T_{pw+} @1 GHz.
15. Device to device skew is measured between outputs under identical transition @ 1 GHz.
16. Additive RMS jitter with 50% duty cycle clock signal.
17. Additive peak-to-peak data dependent jitter with input NRZ data (PRBS $2^{23}-1$).
18. V_{INPP} (MAX) cannot exceed $V_{CC} - V_{EE}$. Input voltage swing is a single-ended measurement operating in differential mode.

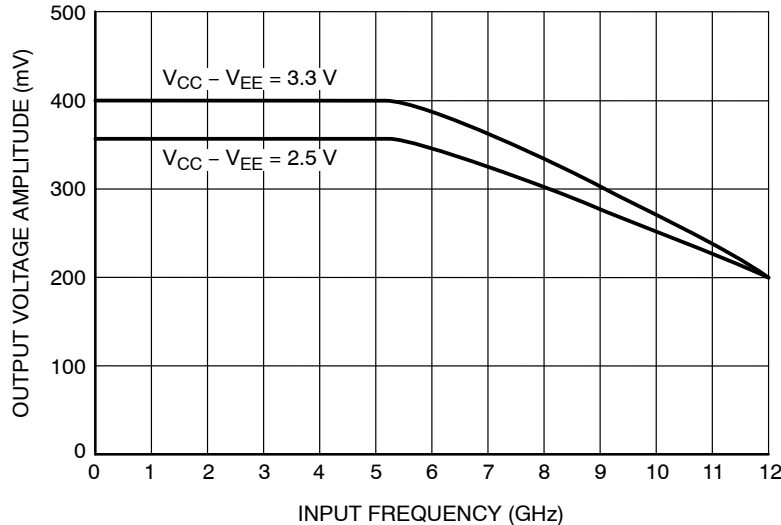


Figure 7. Output Voltage Amplitude (V_{OUTPP}) versus Input Clock Frequency (f_{in}) at Ambient Temperature (Typical)

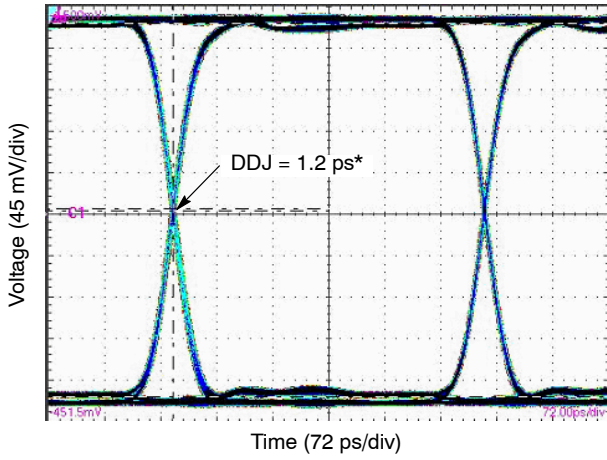


Figure 8. Typical Output Waveform at 2.488 Gb/s with PRBS $2^{23}-1$ ($V_{inpp} = 75$ mV)

*Input signal DDJ = 10 ps

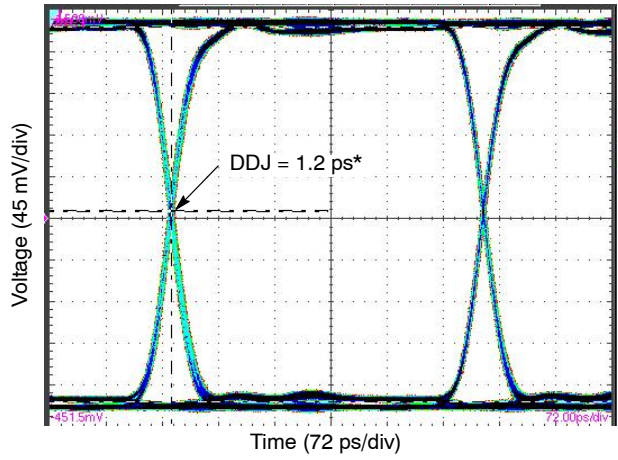


Figure 9. Typical Output Waveform at 2.488 Gb/s with PRBS $2^{23}-1$ ($V_{inpp} = 400$ mV)

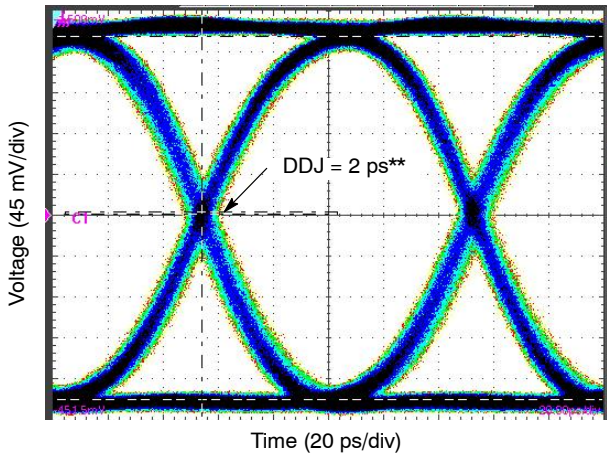


Figure 10. Typical Output Waveform at 10 Gb/s with PRBS $2^{23}-1$ ($V_{inpp} = 75$ mV)

**Input signal DDJ = 12 ps

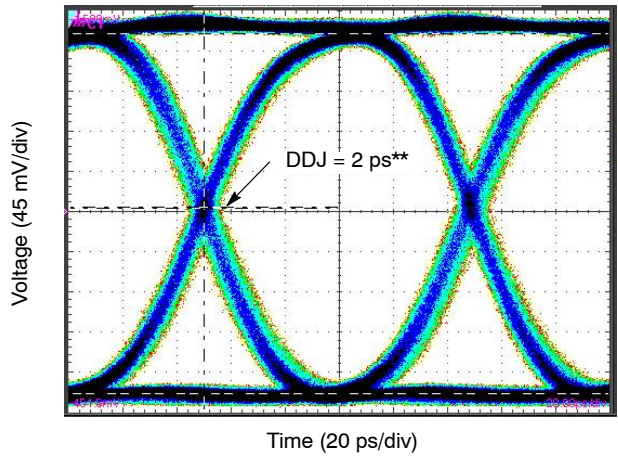


Figure 11. Typical Output Waveform at 10 Gb/s with PRBS $2^{23}-1$ ($V_{inpp} = 400$ mV)

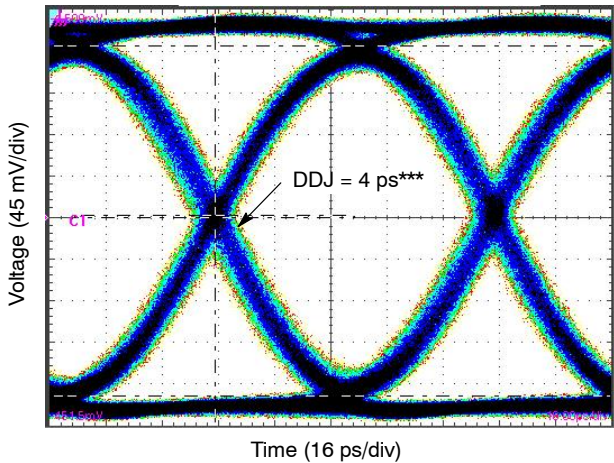


Figure 12. Typical Output Waveform at 12 Gb/s with PRBS $2^{23}-1$ ($V_{inpp} = 75$ mV)

***Input signal DDJ = 14 ps

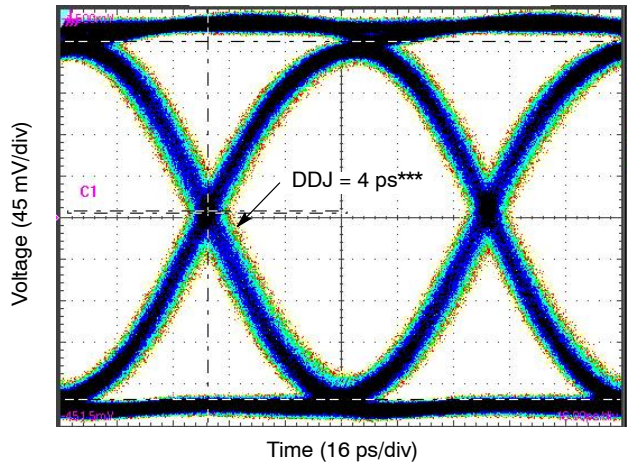


Figure 13. Typical Output Waveform at 12 Gb/s with PRBS $2^{23}-1$ ($V_{inpp} = 400$ mV)

NB7L86M

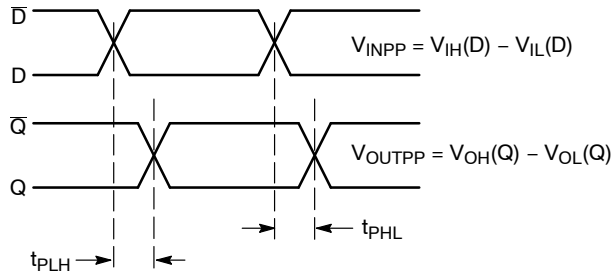


Figure 14. AC Reference Measurement

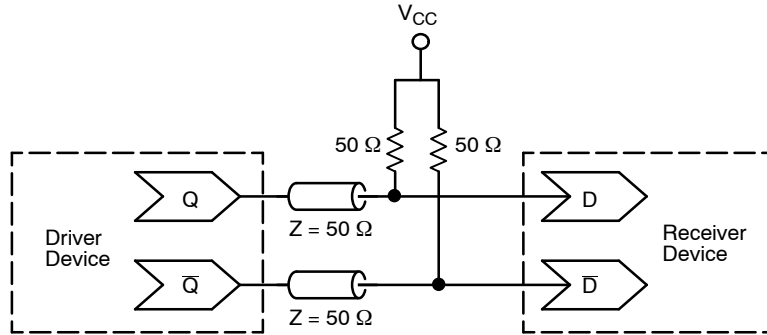


Figure 15. Typical Termination for Output Driver and Device Evaluation (Refer to Application Note AND8173 – Termination and Interface of ON Semiconductor of ECL Logic Devices with CML Output Structure)

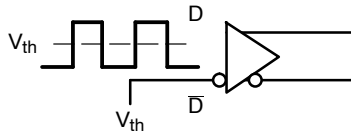


Figure 16. Differential Input Driven Single-Ended

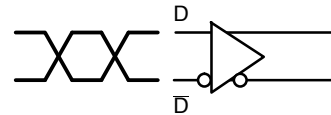


Figure 17. Differential Inputs Driven Differentially

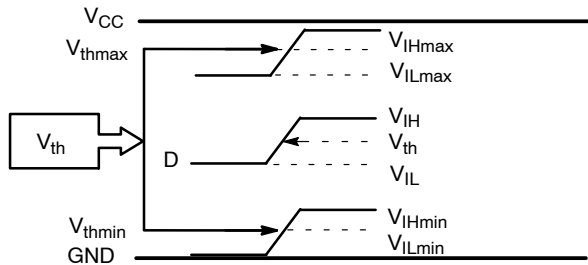


Figure 18. V_{th} Diagram

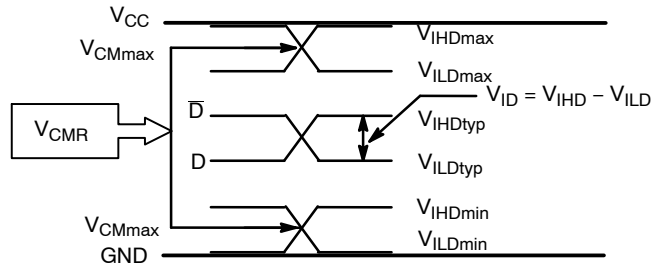


Figure 19. V_{CMR} Diagram

NB7L86M

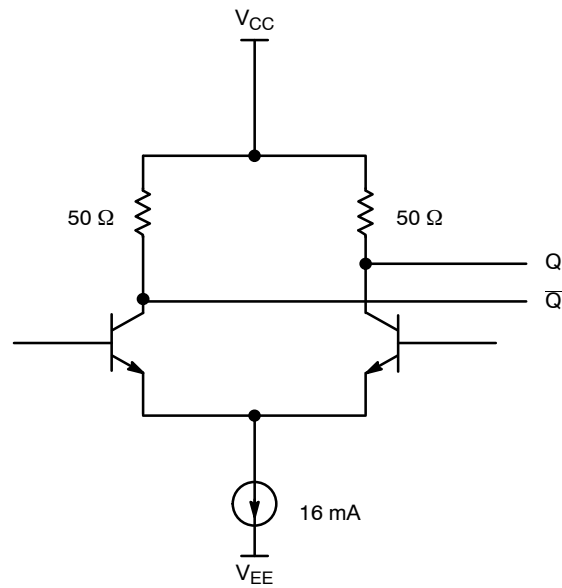


Figure 20. CML Output Structure

Table 10. INTERFACING OPTIONS

| INTERFACING OPTIONS | CONNECTIONS |
|---------------------|--|
| CML | Connect VTD0, $\overline{VTD0}$, VTD1, $\overline{VTD1}$, VTSEL to V_{CC} |
| LVDS | Connect VTD0, $\overline{VTD0}$ together for D0 input. Connect VTD1, $\overline{VTD1}$ together for D0 input. Leave VTSEL open for SEL input. |
| AC-COUPLED | Bias VTD0, $\overline{VTD0}$, VTSEL and VTD1, $\overline{VTD1}$ Inputs within (V_{CMR}) Common Mode Range |
| RSECL, LVPECL | Standard ECL Termination Techniques. See AND8020/D. |
| LVTTTL, LVCMOS | An external voltage should be applied to the unused complementary differential input. Nominal voltage 1.5 V for LVTTTL and $V_{CC}/2$ for LVCMOS inputs. |

NB7L86M

Application Information

All inputs can accept PECL, CML, and LVDS signal levels. The input voltage can range from V_{CC} to 1.2 V.

Examples interfaces are illustrated below in a 50 Ω environment ($Z = 50 \Omega$).

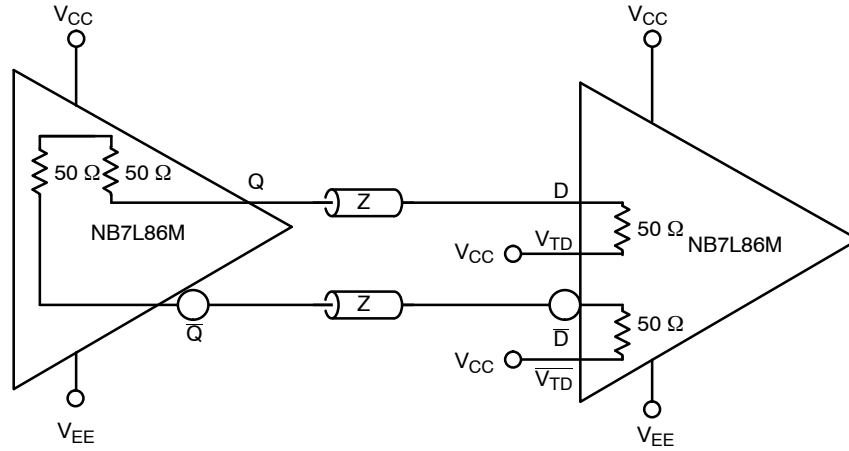


Figure 21. CML to CML Interface

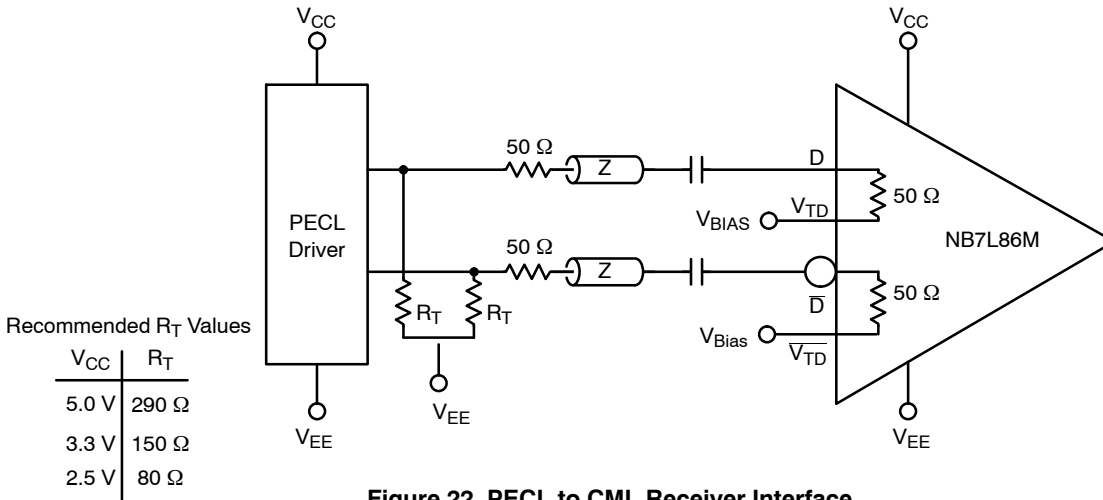


Figure 22. PECL to CML Receiver Interface

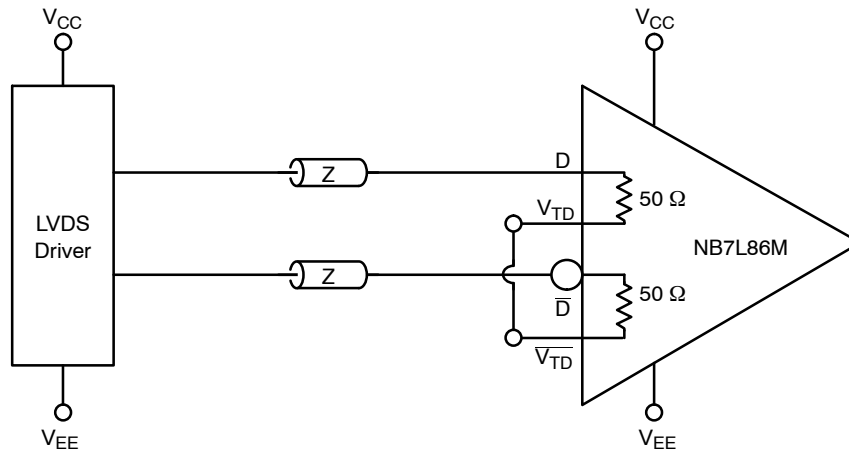


Figure 23. LVDS to CML Receiver Interface

NB7L86M

ORDERING INFORMATION

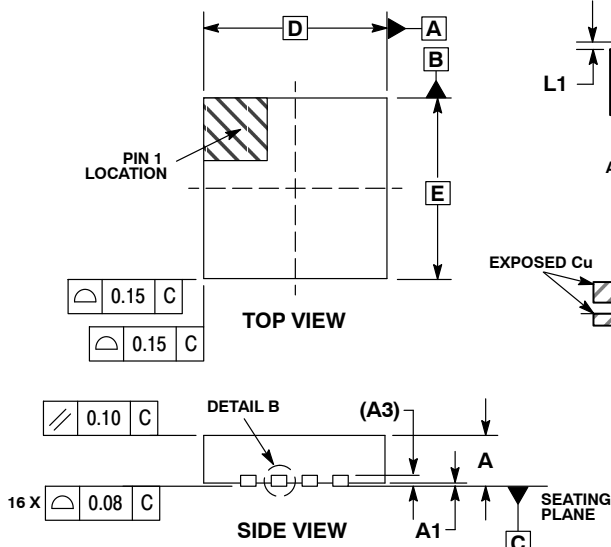
| Device | Package | Shipping† |
|--------------|---------------------|------------------|
| NB7L86MMN | QFN-16 | 123 Units/Rail |
| NB7L86MMNG | QFN-16 (Pb-Free) | 123 Units/Rail |
| NB7L86MMNR2 | QFN-16 | 3000 Tape & Reel |
| NB7L86MMNR2G | QFN-16 (Pb-Free) | 3000 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NB7L86M

PACKAGE DIMENSIONS

16 PIN QFN CASE 485G-01 ISSUE D

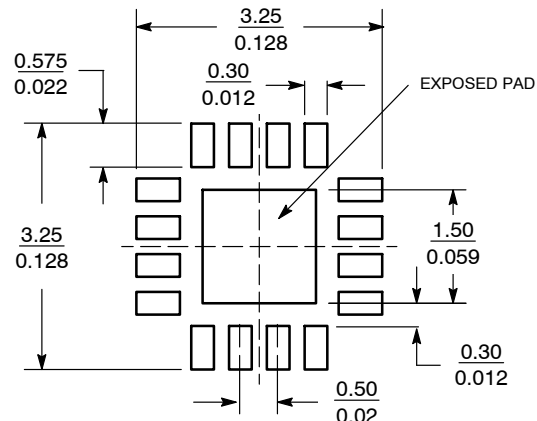
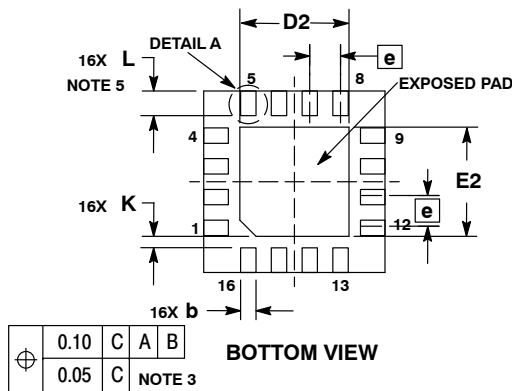


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 | REF |
| b | 0.18 | 0.30 |
| D | 3.00 | BSC |
| D2 | 1.65 | 1.85 |
| E | 3.00 | BSC |
| E2 | 1.65 | 1.85 |
| e | 0.50 | BSC |
| K | 0.18 | TYP |
| L | 0.30 | 0.50 |
| L1 | 0.00 | 0.15 |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

The products described herein (NB7L86M), may be covered by U.S. patents including 6,362,644. There may be other patents pending.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative